What is claimed is:

1. A multiple operating system control apparatus for a multiple operating system having plural operating systems executed in a digital arithmetic processor and including a first operating system and a second operating system and a plurality of pieces of hardware, each piece of hardware assigned to a corresponding operating system, comprising:

respective pieces of hardware having assigned interrupt numbers stored in a table so as to maintain the operating systems independent from each other;

the digital arithmetic processor programmed to alternately switch, under inter-operating system control software control, on the basis of said table, between and said first and second operating systems to alternately execute said first and second operating systems; and

an interrupt number or an input and output address used by said second operating system for said first operating system when starting said first operating system being reserved.

2. The multiple operating system control apparatus of Claim 1,

wherein each of said first and second operating systems include a conversion table used by said digital arithmetic processor for converting a virtual memory address to a physical address; and

said digital arithmetic processor is programmed to include a procedure for directing said digital arithmetic processor to use the conversion table for an operating system to be executed after switching is executed when selecting and switching an operating system, which is called as a interrupt processing routine or called by said first and second operating systems individually when an interrupt occurs,

3. The multiple operating system control apparatus of Claim 1, and further comprising:

a. said digital arithmetic processor having a priority level for each individual operating system of said plural operating systems during operation;

b. said digital arithmetic processor being programmed to preferentially execute a program on a high priority operating system by:

i. not switching the high priority operating system to an operating system with a lower priority level, or

ii. switching the high priority operating system to an operating system lower in priority for a definite time interval and then switching back to the operating system with a high priority.

4. The multiple operating system control apparatus according to claim 1, wherein the interrupt table is divided into two so as to separately use them for the operating systems, the interrupt table being switched from one of the two to the other thereof when an interrupt occurs.

5. The multiple operating system control apparatus according to claim 1, wherein I/O addresses assigned respectively to the pieces of hardware are stored in the table so as to maintain the operating systems independent of each other.

6. The multiple operating system control apparatus according to claim 5, and further including an interrupt controller and a timer and wherein the inter-operating system control software accepts an interrupt from said interrupt controller and an interrupt from said timer.

7. The multiple operating system control apparatus according to claim 6, wherein the inter-operating system control software causes one of the operating systems to be assigned more preferentially than the other.

8. The multiple operating system control apparatus according to claim 7, wherein the other of the operating systems is operated as a device driver.

9. The multiple operating system control apparatus according to claim 8, wherein the operating systems and the inter-operating system control software are operated in a privileged mode, but a program is not.

10. An apparatus comprising: /

a. a digital arithmetic processor having at least a first operating system and a second operating system operating therein, said processor having inter-operating system control software to switch therebetween;

b. a plurality of pieces of hardware, each piece of hardware assigned to a corresponding operating system, with respective pieces of hardware having assigned interrupt numbers stored in a table so as to maintain the operating systems independent from each other.

11. The apparatus of Claim 10 wherein:

the digital arithmetic processor is programmed to alternately switch, under inter-operating system control software control, on the basis of said table, between and said first and second operating systems to alternately execute said first and second operating systems; and

an interrupt number or an input and output address used by said second operating system for said first operating system when starting said first operating system is reserved.

12. The apparatus of Claim 11, wherein:

wherein each of said first and second operating systems include a conversion table used by said digital arithmetic processor for converting a virtual memory address to a physical address; and

said digital arithmetic processor is programmed to include a procedure for directing said digital arithmetic processor to use the conversion table for an operating system to be executed after switching is executed when selecting and switching an operating system, which is called as a interrupt processing routine or called by said first and second operating systems individually when an interrupt occurs,

13. The apparatus of Claim 10, and further comprising:

a. said digital arithmetic processor having a priority level for each individual operating system of said plural operating systems during operation;

b. said digital arithmetic processor being programmed to preferentially execute a program on a high priority operating system by:

i. not switching the high priority operating system to an operating system with a lower priority level, or

ii. switching the high priority operating system to an operating system lower in priority for a definite time interval and then switching back to the operating system with a high priority.

14. The apparatus according to claim 10, wherein the interrupt table is divided into two so as to permit separate use for the operating systems, the interrupt table being switched from one of the two to the other thereof when an interrupt occurs.

15. The apparatus according to claim 10, wherein I/O addresses assigned respectively to the pieces of hardware are stored in the table so as to maintain the operating systems independent of each other.

16. The apparatus according to claim 10, and further in including an interrupt controller and a timer and wherein the inter-operating system software accepts an interrupt from said interrupt controller and an interrupt from said timer.

17. The apparatus according to claim 16, wherein the inter-operating system software causes one of the operating systems to be assigned more preferentially than the other.

18. The apparatus according to claim 17, wherein the other of the operating systems is operated as a device driver.

19. The apparatus according to claim 18, wherein the operating systems and the inter-operating system control software are operated in a privileged mode, but a program is not.

20. A multiple operating system comprising: /

a. a digital arithmetic processor having plural operating systems executed therein including a first operating system and a second operating system;

b. and a plurality of pieces of hardware, each piece of hardware assigned to a corresponding operating system, said respective pieces of hardware having assigned interrupt numbers;

c. a table storing said assigned interrupt numbers so as to maintain the operating systems independent from each other, the digital arithmetic processor programmed to alternately switch, under inter-operating system control software control, on the basis of said table, between and said first and second operating systems to alternately execute said first and second operating systems; and

d. an interrupt number or an input and output address used by said second operating system for said first operating system when starting said first operating system being reserved.

21. The multiple operating system of Claim 20 and further including:

a conversion table for converting a virtual memory address to a physical address included in each of said first and second operating systems.

22. The multiple operating system of Claim 20 wherein:

said digital arithmetic processor is programmed to include a procedure for directing said digital arithmetic processor to use the conversion table for an operating system to be executed after switching is executed when selecting and switching an operating system, which is called as a interrupt processing routine or called by said first and second operating systems individually when an interrupt occurs,

23. The multiple operating system of Claim 20, wherein:

a. said digital arithmetic processor has a priority level for each individual operating system of said plural operating systems during operation;

b. said digital arithmetic processor is programmed to preferentially execute a program on a high priority operating system by:

i. not switching the high priority operating system to an operating system with a lower priority level, or

ii. switching the high priority operating system to an operating system lower in priority for a definite time interval and then switching back to the operating system with a high priority.

24. The multiple operating system according to claim 20, wherein the interrupt table is divided into two so as to separately use them for the operating systems, the interrupt table being switched from one of the two to the other thereof when an interrupt occurs.

25. The multiple operating system according to claim 20, wherein I/O addresses assigned respectively to the pieces of hardware are stored in the table so as to maintain the operating systems independent of each other.

26. The multiple operating system according to claim 25, and further including an interrupt controller and a timer and wherein the inter-operating system control software accepts an interrupt from said interrupt controller and an interrupt from said timer.

27. The multiple operating system according to claim 26, wherein the inter-operating system control software causes one of the operating systems to be assigned more preferentially than the other.

28. The multiple operating system according to claim 27, wherein the other of the operating systems is operated as a device driver.

29. The multiple operating system according to claim 28, wherein the operating systems and the inter-operating system control software are operated in a privileged mode, but a program is not.

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